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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,242	03/29/2004	Chad Thomas Steward	55123P298	2207

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EXAMINER	
YOUNG, BRIAN K	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,242	STEWARD ET AL.	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~3/29/04~~. 8/23/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-26 are rejected under 35 U.S.C. 102(a) as being anticipated by applicants admitted prior art.

Regarding claims 1,12,20 and 22 applicant's admitted prior art teaches (fig.1) a successive approximation analog-to-digital converter comprising: an analog sample and hold circuit (ANALOG INPUT SAMPLE AND HOLD); a switched capacitor DAC having an input coupled to an output of the sample and hold circuit (SWITCHED CAPACITOR DAC); comparator having an input coupled to an output of the switched capacitor DAC (COMPARATOR); a plurality of set-reset latches, each set-reset latch being responsive to a combination of control signals and the output of the comparator and providing non-overlapping switch driver signals as set-reset latch outputs (SAR and NON-OVERLAPPING SWITCH DRIVERS); the switch driver signals being coupled to control the switched capacitor DAC.

In regards to claims 2-11,13-19,21, and 23-26 figure 1 teaches that the switched capacitor DAC is a differential switched capacitor controlled by a state machine (STATE MACHINE). Also that the set-reset latches have switch driver signal outputs that are level shifted and the output comparison to the combination of control signals the comparator, and that the set-reset latches are NOR and NAND gate based latches. The term "hybrid logic" is ambiguous as are the terms "positive" and "negative" logic.

Page 1 of the specification recites "a traditional successive approximation (SAR) analog-to- digital converter (ADC) shown schematically shown in Figure 1 uses a differential switched capacitor DAC coupled to a comparator having an output coupled to a successive approximation register controlling non-overlapping switch drivers coupled to the switched capacitor DAC. An analog input sample-and-hold is provided, which may be the overall SAR ADC switched capacitor DAC itself, with the being controlled by some form controller such as the state machine shown.
In a switched capacitor DAC, the capacitor values may be in a binary sequence (radix with one terminal of all capacitors connected to the DAC output. (Reduced radix and mixed radix DACS are also known)."

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Pilost discloses (fig.4) an SAR ADC FIG. 4 the ADC encoder having logic device 22. The output of comparator 20 is connected to one of the inputs of N AND circuits A.sub.0, A.sub.1, . . . , A.sub.N-1. The second inputs of AND circuits A.sub.0 through A.sub.N-1, the so-called clock inputs and designated by CLK'.sub.0, CLK'.sub.1, . . . , CLK'.sub.N-1 are scanned from top to bottom by a clock pulse. The output of circuit A.sub.0 is connected to the reset input (R) of a flip-flop FF.sub.0, the sign flip-flop. The set input (S) of flip-flop FF.sub.0 is connected to an initiating line INIT. This line is also connected to one of the inputs of a set of OR logic circuits OR1, OR2, . . . OR.sub.N-1. The second input of each of these OR circuits is connected to the output of one of the AND circuits A.sub.1 through A.sub.N-1. The output of each of these OR circuits OR.sub.1 through OR.sub.N-1 is connected to the input(s) of the flip-flop circuits

FF.sub.1, FF.sub.2, . . . FF.sub.N-1. The reset inputs of flip-flop circuit FF.sub.1 through FF.sub.N-1 are connected to inputs CLK'.sub.0 through CLK'.sub.N-2, respectively. Finally, a direct line is connected to a voltage source +V so as to supply a bit equal to "1" (bit kN, of binary word X.sub.(n), in a permanent manner. The normal logic outputs of flip-flop circuits FF.sub.0 through FF.sub.N-1 as well as line k.sub.N =1 which is maintained to logic level 1, in a permanent manner, are connected to the inputs of the D/A converter 24 the output of which is connected to one of the two inputs of the comparator 20. The set of flip-flop circuits (FF.sub.0, FF.sub.1, . . . , FF.sub.N-1) comprises the output register (ADC REG) of the analog-to-digital converter according to this invention. This register is intended to contain the N significant bits looked for. Said N bits, more particularly, include the so-called sign bit in flip-flop FF.sub.0. During the successive approximation converting process, the N most significant bits in each (N+1) bit rounded-off value, will be stored in the output register.

Somayajula discloses (fig.6c) an SAR ADC having a return path for use in a switched capacitor circuit that includes an array of capacitors and a plurality of switches for selectively coupling voltages to capacitors. A set of latches selectively controls the plurality of switches during time periods partitioned into non-overlapping reset and set cycles. During a first such time period, a selected one of the capacitors is decoupled from a current voltage during the reset cycle and coupled to a selected reference voltage during the set cycle.

Jones et al disclose another example of a traditional SAR ADC.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

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